

What Is Claimed Is:

- 1 1. An ESD protection component, comprising:  
2 at least two MOS field effect transistors (FETs) of a first  
3 conductivity type, having two gates and formed in parallel  
4 on a first semiconductive layer having a second conductivity  
5 type;  
6 a first well having a first conductivity type, formed on  
7 the first semiconductive layer, comprising:  
8 a connecting area, formed between the MOS FETs;  
9 two parallel extension areas, formed perpendicular to  
10 the gates of the MOS FETs; and  
11 a first doping area of the second conductivity type,  
12 formed in the connecting area.
- 1 2. The ESD protection component in claim 1, wherein the ESD  
2 protection component further comprises a guard ring of the  
3 second conductivity type.
- 1 3. The ESD protection circuit in claim 2, wherein the first  
2 conductive layer is connected to a power supply through the  
3 guarding ring.
- 1 4. The ESD protection circuit in claim 1, wherein the first well  
2 is separated from the drains of the MOS FETs.
- 1 5. The ESD protection circuit in claim 1, wherein each of the  
2 MOS FETs has a source region of the first conductivity type,  
3 coupled to a power rail.

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- 1 6. The ESD protection circuit in claim 1, wherein the first well  
2 is coupled to a pad through the extension areas.
- 1 7. The ESD protection circuit in claim 1, wherein the first  
2 doping region is coupled to a pad.
- 1 8. The ESD protection circuit in claim 1, wherein each of the  
2 MOS FETs has a drain region of the first conductivity type  
3 coupled to a pad.
- 1 9. An ESD protection component, comprising:  
2 at least two MOS field effect transistors (FETs) of a first  
3 conductivity type, comprising:  
4 two gates, formed in parallel on a first semiconductive  
5 layer having a second conductivity type;  
6 two sources of the first conductivity type, coupled to a  
7 power supply; and  
8 two drains of the first conductivity type;  
9 a first well having a first conductivity type, formed on  
10 the first semiconductive layer, comprising:  
11 a connecting area, formed between the MOS FETs;  
12 Two parallel extension areas, formed perpendicular to  
13 the gates of the MOS FETs; and  
14 a first doping area of the second conductivity type,  
15 formed in the connecting area, and coupled to a pad; and  
16 a guard ring of the second conductivity type, formed  
17 on the first semiconductive layer, coupled to the power  
18 supply;  
19 wherein the first well is coupled to the pad through the  
20 extension areas.